AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the above-referenced application.

Listing of Claims:

Claims 1 - 11 (Cancelled)

12. (Currently amended) A method of manufacturing a complementary integrated circuit, comprising:

preparing a semiconductor substrate;

forming a region for forming an n-channel element and a region for forming a p-channel element on said semiconductor substrate via an element isolation region;

forming a dummy gate electrode in each of said region for forming an [[n-cannel]] n-channel element and said region for forming a p-channel element;

forming n-type diffusion regions in said region for forming an n-channel element and forming p-type diffusion regions in said region for forming a p-channel element, wherein said n-type diffusion regions are formed by implanting an n-type impurity into said region for forming an n-channel element by using a first mask, said first mask including: (1) said dummy gate formed in said region for forming an n-channel element and (2) a first resist film covering said region for forming a p-channel element, and wherein said p-type diffusion regions are formed by implanting a p-type impurity into said region for forming a p-channel element by using a second mask, said second mask including: (1) said dummy gate formed in said region for forming a p-channel element and (2) a second resist film covering said region for forming an n-channel element;

forming an insulating film over the entire surface of said semiconductor substrate;

removing said dummy gate formed in one of said region for forming an n-channel element and said region for forming a p-channel element to form a first trench in said insulating film;

filling said first trench with a gate electrode material;

removing said dummy gate formed in the other of said region for forming an n-channel element and said region for forming a p-channel element to form a second trench in said insulating film; and

filling said second trench with a gate electrode material.

13. (Cancelled)

14. (Original) A method of manufacturing a complementary integrated circuit according to claim 12, wherein, in said forming an insulating film over the entire surface of said semiconductor substrate, said insulating film is formed so as to cover said dummy gate formed in said region for forming an n-channel element and said dummy gate formed in said region for forming a p-channel element; and said method further comprises, after said forming an insulating film over the entire surface of said semiconductor substrate, removing at least a potion of said insulating film to expose upper surfaces of said dummy gate formed in said region for forming an n-channel element and said dummy gate formed in said region for forming a p-channel element.

15. (Original) A method of manufacturing a complementary integrated circuit according to claim 12, wherein said method further comprises, after said removing said dummy gate formed in one of said region for forming an n-channel element and said region for forming a p-channel element to form a first trench in said insulating film, forming a gate insulating film at the bottom portion of said first trench, wherein, in said filling said first trench with a gate electrode material, said first trench is filled with said gate electrode material within said first trench and on said gate insulating film formed at the bottom portion of said first trench,

wherein said method further comprises, after said removing said dummy gate formed in the other of said region for forming an n-channel element and said region for forming a p-channel element to form a second trench in said insulating film, forming a gate insulating film at the bottom portion of said second trench, and wherein, in said filling said second trench with a gate electrode material, said second trench is filled with said gate electrode material within said second trench and on said gate insulating film formed at the bottom portion of said second trench.

16. (Original) A method of manufacturing a complementary integrated circuit according to claim 12, wherein, in said filling said first trench with a gate electrode material, a film made of said gate electrode material is formed on whole surface of said semiconductor substrate so as to fill said first trench and is polished to expose the upper surface of said insulating film, and

wherein, in said filling said second trench with a gate electrode material, a film made of said gate electrode material is formed on whole surface of said semiconductor substrate so as to fill said second trench and is polished to expose the upper surface of said insulating film.

17. (Original) A method of manufacturing a complementary integrated circuit according to claim 12, wherein a gate electrode material portion filling a trench formed in said region for forming an n-channel element among said first trench and said second trench comprises a metal material which has a work function close to the work function of n-type polysilicon at least at a bottom portion of said gate electrode material portion, and

wherein a gate electrode material portion filling a trench formed in said region for forming a p-channel element among said first trench and said second trench comprises a metal material which has a work function close to the work function of p-type polysilicon at least at a bottom portion of said gate electrode material portion.

18. (Currently amended) A method of manufacturing a complementary integrated circuit ~~according to claim 12~~, comprising:

preparing a semiconductor substrate;

forming a region for forming an n-channel element and a region for forming a p-channel element on said semiconductor substrate via an element isolation region;

forming a dummy gate electrode in each of said region for forming an n-channel element and said region for forming a p-channel element;

forming n-type diffusion regions in said region for forming an n-channel element and forming p-type diffusion regions in said region for forming a p-channel element;

forming an insulating film over the entire surface of said semiconductor substrate;

removing said dummy gate formed in one of said region for forming an n-channel element and said region for forming a p-channel element to form a first trench in said insulating film;

filling said first trench with a gate electrode material;

removing said dummy gate formed in the other of said region for forming an n-channel element and said region for forming a p-channel element to form a second trench in said insulating film; and

filling said second trench with a gate electrode material;

wherein a gate electrode material portion filling a trench formed in said region for forming an n-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, a material selected from a group consisting of zirconium and hafnium, and

wherein a gate electrode material portion filling a trench formed in said region for forming an p-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, a material selected from a group consisting of platinum silicide, iridium silicide, cobalt, nickel, rhodium, palladium, rhenium and gold.

19. (Original) A method of manufacturing a complementary integrated circuit according to claim 12, wherein a gate electrode material portion filling a trench formed in said region for forming an n-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, n-type polysilicon deposited while doping n-type impurity, and

wherein a gate electrode material portion filling a trench formed in said region for forming a p-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, p-type polysilicon deposited while doping p-type impurity.

20. (Original) A method of manufacturing a complementary integrated circuit according to claim 12, wherein a gate electrode material portion filling a trench formed in said region for forming an n- channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, a material having a work function close to the work function of n-type polysilicon and other portion of said gate electrode material portion comprises a material having a predetermined low electrical resistivity, and

wherein a gate electrode material portion filling a trench formed in said region for forming a p-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, a material having a work function close to the work function of p-type polysilicon and other portion of said gate electrode material portion comprises a material having a predetermined low electrical resistivity.

21. (Original) A method of manufacturing a complementary integrated circuit, comprising:

preparing a semiconductor substrate;

forming a region for forming an n-channel element and a region for forming a p-channel element on said semiconductor substrate via an element isolation region;

forming an insulating film over the entire surface of said semiconductor substrate;

selectively removing said insulating film to form a first trench in said insulating film on one of said region for forming an n-channel element and said region for forming a p-channel element;

filling said first trench with a gate electrode material;

selectively removing said insulating film to form a second trench in said insulating film on the other of said region for forming an n-channel element and said region for forming a p-channel element;

filling said second trench with a gate electrode material;

removing said insulating film;

forming n-type diffusion regions in said region for forming an n-channel element and forming p-type diffusion regions in said region for forming a p-channel element.

22. (Original) A method of manufacturing a complementary integrated circuit according to claim 21, wherein said method further comprises, after said selectively removing said insulating film to form a first trench in said insulating film on one of said region for forming an n-channel element and said region for forming a p-channel element, forming a gate insulating film at the bottom portion of said first trench, wherein, in said filling said first trench with a gate electrode material, said first trench is filled with said gate electrode material within said first trench and on said gate insulating film formed at the bottom portion of said first trench,

wherein said method further comprises, after said selectively removing said insulating film to form a second trench in said insulating film on the other of _said region for forming an n-channel element and said region for forming a p-channel element, forming a gate insulating film at the bottom portion of said second trench, and wherein, in said filling said second trench with a gate electrode material, said second trench is filled with said gate electrode material within said second trench and on said gate insulating film formed at the bottom portion of said second trench.

23. (Original) A method of manufacturing a complementary integrated circuit according to claim 21, wherein, in said filling said first trench with a gate electrode material, a film made of said gate electrode material is formed on whole surface of said semiconductor substrate so as to fill said first trench and is polished to expose the upper surface of said insulating film, and

wherein, in said filling said second trench with a gate electrode material, a film made of said gate electrode material is formed on whole surface of said semiconductor substrate so as to fill said second trench and is polished to expose the upper surface of said insulating film.

24. (Original) A method of manufacturing a complementary integrated circuit according to claim 21, wherein a gate electrode material portion filling a trench formed in said region for forming an n-channel element among said first trench and said second trench comprises a metal material which has a work function close to the work function of n-type polysilicon at least at a bottom portion of said gate electrode material portion, and

wherein a gate electrode material portion filling a trench formed in said region for forming a p-channel element among said first trench and said second trench comprises a metal material which has a work function close to the work function of p-type polysilicon at least at a bottom portion of said gate electrode material portion.

25. (Original) A method of manufacturing a complementary integrated circuit according to claim 21, wherein a gate electrode material portion filling a trench formed in said region for forming an n-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, a material selected from a group consisting of zirconium and hafnium, and

wherein a gate electrode material portion filling a trench formed in said region for forming an p-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, a material selected from a group consisting of platinum silicide, iridium silicide, cobalt, nickel, rhodium, palladium, rhenium and gold.

26. (Original) A method of manufacturing a complementary integrated circuit according to claim 21, wherein a gate electrode material portion filling a trench formed in said region for forming an n-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, n-type polysilicon deposited while doping n-type impurity, and

wherein a gate electrode material portion filling a trench formed in said region for forming a p-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, p-type polysilicon deposited while doping p-type impurity.

27. (Original) A method of manufacturing a complementary integrated circuit according to claim 21, wherein a gate electrode material portion filling a trench formed in said region for forming an n-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, a material having a work function close to the work function of n-type polysilicon and other portion of said gate electrode material portion comprises a material having a predetermined low electrical resistivity, and

wherein a gate electrode material portion filling a trench formed in said region for forming a p-channel element among said first trench and said second trench comprises, at least at a bottom portion thereof, a material having a work function close to the work function of p-type polysilicon and other portion of said gate electrode material portion comprises a material having a predetermined low electrical resistivity.